|  |  |  |  |
| --- | --- | --- | --- |
| EWULogo.png | | **EAST WEST UNIVERSITY** | |
| **Department of Computer Science and Engineering** | |
| **B.Sc. in Computer Science and Engineering Program** | |
| **Mid Term II Examination, Summer 2021** | |
| **Course:** | | **CSE360 – Computer Architecture, Section 3** | |
| **Instructor:** | | **Md. Nawab Yousuf Ali, PhD, Professor, CSE Department** | |
| **Full Marks:** | | **25** | |
| **Time:** | | **1 Hour 20 Minutes** | |
| **Note:** There are FIVE questions, answer ALL of them. Course Outcome (CO), Cognitive Levels and Mark of each question are mentioned at the right margin. | | | |
| 1. | A four-way set-associative cache has lines of 32 bytes and a total size of 16 KB. The 256-MB main memory is byte addressable. What is the format of main memory addresses? | | [ CO2, C3, Mark: 3] |
| 2. | Consider a memory system with the following parameters:  Tc = 160 ns Cc = 10^-6 $/ bit  Tm = 1100 ns Cm = 10^-7 $/ bit  a) What is the cost of 3.5 MByte of main memory using cache memory technology?  b) If the effective access time is 3% greater than the main memory access time, what is the hit ratio H? | | [CO2, C3, Mark:1+3] |
| 3. | Consider a hard disk drive having the following specifications   |  |  | | --- | --- | | Rotational speed | 5000 RPM | | Transfer rate | 50 MB/sec | | Average seek time | 35 milliseconds | | Controller overhead | 2.5ms |  1. Calculate the average rotational latency. 2. What is the average time to read 2.5 KB of data? | | [ CO2, C5, Mark:1+3] |
| 4. | Consider a magnetic disk drive with 10 **double sided** magnetic disks inside it. Upper surface of every disk contains 150 tracks and lower surface only has 100 tracks. Each track has 100 sectors where sector size is 2kbytes. Suppose average seeks time is 5.5 ms, track-to-track access time is 1ms and drive rotates at 4,000 rmp.  a) Calculate the size of the magnetic disk drive.  b) Find the average access time. c) What is the total time needed to transfer a 10 MB file from the drive. | | [CO2, C3, Mark: 2+2+3] |
| 5. | Examination of the timing diagram of the 8237A indicates that once a block transfer begins, it takes six bus clock cycles per DMA cycle. During the DMA cycle, the 8237A transfers one byte of information between memory and I/O devices   1. Suppose we clock the 8237A at a rate of 3.5 MHz. How long does it take to transfer one byte? 2. What would be the maximum attainable data transfer rate? 3. Assume that the memory is not fast enough and we have to insert four wait states per DMA cycle. What will be the actual data transfer rate? | | [ CO2, C3, Mark: 2+2+3] |